Nuclear Pulse Height Measurement Using FPGA Techniques

P.C. Tsao and H.P. Chou

Abstract–The present work is to use FPGAs as a digital processor for pulse height measurement. A digital periodic triangle signal is generated by an up-down counter with a positive edge trigger and followed by a synthesizable digital to analog converter (DAC) to generate pulse height information directly. The present pulse height processor is further connected to a personal digital assistant (PDA) to use as a portable spectrometer for field use as a simple nuclide identification tool.

I. Introduction

Many methods for processing nuclear data with digital signal processing technique have been proposed.[1-2]. The field programmable gate array (FPGA) is a digital device and is also proposed to be suitable for digital signal processing. The present work proposed an architecture shown in Fig.1 to measure the pulse height of nuclear radiation signals.

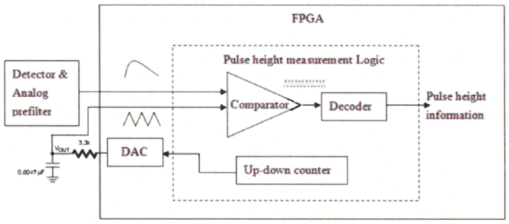

Fig.1. The architecture of the digital processor for pulse height measurement

The analog input is directly connected to the FPGA input pins. A periodic reference triangular signal can be generated by an up-down counter followed by a synthesizable digital to analog converter (DAC). The differential input buffer is used as a comparator to generate logic transitions inside the FPGA when the reference triangular signal across the input voltage levels. According to the characterization of the triangle signal, the transition points are directly decoded to the height information by the decoder.

In modern FPGA devices, differential input buffers are good comparators within a sufficiently large range of input voltage levels, since they are designed to be compatible with various differential signaling standards. Many comparator-based measurement methods using FPGAs are achievable. For example, with the ramping-comparing scheme [1], is suitable for applications with large channel count of relatively slow signals. With Wilkinson rundown scheme [2, 3], charge integration of narrow pulse can be combined with the digitization, although more external analog circuits are needed. With the delta-sigma scheme [4, 5], the signal can be tracked promptly yielding smaller digitization errors at a cost of higher FPGA resource usage. The scheme we studied here is similar to ramping-comparing scheme, but we use digital devices to generate reference signals. Unlikely the passive RC network needs to derive, the measurement logic we used can directly get the input height information. If meshing with high precision DAC, the accuracy can be further improved.

II. The Pulse Height Measuerment Logic

The pulse height measurement logic consists of an up-down counter, a comparator, and a decoder. A digital periodic triangle signal shown in Fig.2 is used as a voltage level reference.

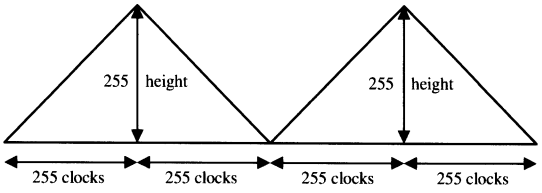

Fig.2. Up-down counter for triangular reference signal generation

The triangular signal is generated by an up-down counter with a positive edge trigger and followed by a synthesizable digital to analog converter (DAC). The up-down counter starts on the up counter and counting down when counting up to 255, so the 256^{th} clock is 254. Vice versa, The up-down counter counts up when the down counter reach to 1, so the 511^{th} clock is 1. The DAC then converts the up-down counts into a triangular waveform as a reference signal for comparison with the voltage impulse.

The comparator makes a transition (0→1 or 1→0) when the triangle signal across the impulse. According to the characterization of the triangle signal, we can directly get the height information at the transition points. For example, the pulse height is a digital number 4 if the transition occurs at the 4^{th} up-down counter clock; the height is a digital number 254 if the transition occurs at the 256^{th} up-down counter clock in 8-bits resolution. The decoder decodes the transition points corresponding to the height information. As shown in Fig.3, the red crosses are transition points with its digital number

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outputs corresponding to the height information determined by clock counts.

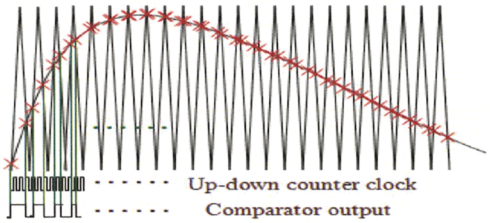

Fig.3. Illustration of the process for pulse height measuring operation

III. SPECIFICATION

The digital to analog converter (DAC) with a 8-bit binary input and a 160MHz system clock works as pulse width modulation (PWM) theory. The output voltage can be set from 0V to 3.3V, where 3.3V is the supply voltage applied to the FPGA I/O bank. The DAC converts a binary number into a voltage directly proportional to the duty cycle of the DAC output. As shown in Fig.4, big binary number (hexadecimal number 80) has bigger duty cycle than small binary number (hexadecimal number 55). The voltage can be converted according to the duty cycle. In above-mentioned case, hexadecimal number 80 (decimal number 128, half of 255) can be converted to 1.65V (half of 3.3V); hexadecimal number 55 (decimal number 85, third of 255) can be converted to 1.1V (third of 3.3V).

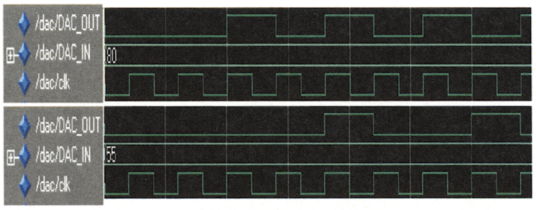

Fig.4. The case for the relationship of different binary input and duty cycle

The output voltage is stable about passing 50 clocks which means settling time is about 0.3125μs, so the period of the analog reference triangle is about 160μs. As shown in Fig.5, the input signal is crossed by the reference voltage twice every 163μs. Use the phase-lock-loop (PLL) clock synthesizer can generate multiphase clock to rise up the resolution, for example, the input signal can be crossed by the reference voltage twice every 41μs in 4-phase 160MHz clock.

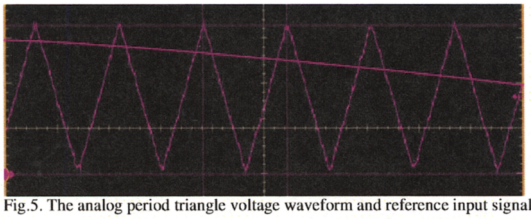

Fig.5. The analog period triangle voltage waveform and reference input signal

IV. TEST RESULTS

Generally we must test by demonstration software running on a computer(PC) or other interface (e.g. a personal digital assistant), but here present a simply way to display height information by the FPGA's seven-segment. According to our specification, the probable digital number is between 0~255. Ideally if the FPGA has enough area, it can immediately display height information by seven-segment continuously. For example, the seven-segment display 166 if the comparator output transition occurs at the 166th up-down counter clock. But considering implement the design in low-cost FPGA, we dividing 0~255 into eight equal parts. The seven-segment display height information refer to Table I.

TABLE I
THE CONTRAST OF SEVEN-SEGMENT DISPLAY

Seven-segment Display	Digital Number	Binary Number
1	0~32	00000000~00100000
2	33~64	00100001~01000000
3	65~96	01000001~01100000
4	97~128	11000001~10000000
5	129~160	10000001~10100000
6	161~192	10100001~11000000
7	193~224	11000001~11100000
8	225~255	11100001~11111111

For example, the seven-segment display 6 if the comparator output transition occurs at the up-down counter clock which is digital number between 161~192 (e.g. 166th or 344th or 676th is all digital number 166). As shown in Fig.6, the transition occurs at the digital number 166 (binary number 10100110), the seven-segment concededly display 6.

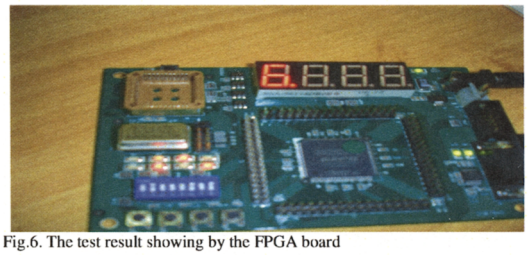

Fig.6. The test result showing by the FPGA board

The display period can be certainly user define, for example, dividing 0~255 into 32 equal parts. It could be modulated depending on the hardware resources.

V. CONCULSION

An inexpensive, portable digital signal processor for pulse height measurement is presented. It is implemented and

processed using the low cost FPGA technique. The pulse height processor can be use with portable spectrometer for field application. Further investigation is under way to develop multi-phase clock to improve the measurement resolution.

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